Notice of Allowability	Application No. 10/708,055	Applicant(s) LIEBMANN ET AL.	
	Examiner Stephen Rosasco	Art Unit 1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Filing and IDS 6/21/04*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALLOWANCE

The following is an examiner's statement of reasons for allowance: the claimed invention is distinguished over the prior art of record in that the prior art does not teach a method of designing a layout of an alternating phase shifting mask for projecting an image of an integrated circuit design comprising: providing a design of an integrated circuit layout having a plurality of features to be projected using alternating phase shifting segments, including a feature having a critical width along a length thereof that extends beyond another feature; providing alternating phase shift design rules based on alternating phase shift design parameters comprising minimum phase width, minimum phase-to-phase spacing, and minimum extension of critical width beyond another feature;

identifying portions of the integrated circuit layout having a critical width feature that violate the alternating phase shift design rules; redesigning the critical width feature in the integrated circuit layout that violates the alternating phase shift design rules by reducing the length that the critical width feature extends beyond the other feature to the minimum extension; and generating an alternating phase shifting mask layout with the reduced length of the critical width feature in conformance with the alternating phase shift design rules.

And wherein the feature having a critical width along a length thereof comprises a gate-shrink region of a transistor, and wherein the other feature is a diffusion region of a transistor.

The applicant discusses the limitations of the prior art - One means of balancing the desire of applying altPSM widely to large portions of the layout, while at the same time containing the altPSM shapes to a simple local environment, is described in the SPIE

publication "Alternating Phase Shifted Mask for Logic Gate Levels, Design and Mask Manufacturing" authored in part by one of the inventors of the instant application. The drawback of the iterative localization described in this publication is the enormous computational effort and resulting long runtimes involved in repeatedly deriving and checking altPSM solutions.

Cote et al. (6,745,372) teach a system that simulates effects of a manufacturing process on an integrated circuit to enhance process latitude and/or reduce layout size. During operation, the system identifies problem areas in the simulated printed image that do not meet a specification. Next, the system moves corresponding shapes in the target layout to produce a new target layout for the integrated circuit, so that a simulated printed image of the new target layout meets the specification.

Liu (6,944,844) teaches a method of determining an impact of line end shortening on a feature, the method comprising: simulating printing of predetermined points on the feature to determine line end shortening; and measuring a critical dimension at a predetermined location on the feature, based on the simulating, wherein the predetermined location is associated with device performance, and wherein the predetermined location is outside an active region associated with the feature.

And wherein the feature implements a gate and the layout distance is coincident with an edge of the active region that implements a diffusion area associated with the gate.

And further including measuring a distance between the simulated printing of evaluation points, wherein the distance is the critical dimension.

And wherein the feature implements a gate and the active region implements a diffusion area associated with the gate.

However, neither reference teaches a method of designing a layout of an alternating phase shifting mask for projecting an image of an integrated circuit design including a feature having a critical width along a length thereof that extends beyond another feature;

providing alternating phase shift design rules based on alternating phase shift design parameters comprising minimum phase width, minimum phase-to-phase spacing, and minimum extension of critical width beyond another feature;

identifying portions of the integrated circuit layout having a critical width feature that violate the alternating phase shift design rules; redesigning the critical width feature in the integrated circuit layout that violates the alternating phase shift design rules by reducing the length that the critical width feature extends beyond the other feature to the minimum extension; and generating an alternating phase shifting mask layout with the reduced length of the critical width feature in conformance with the alternating phase shift design rules.

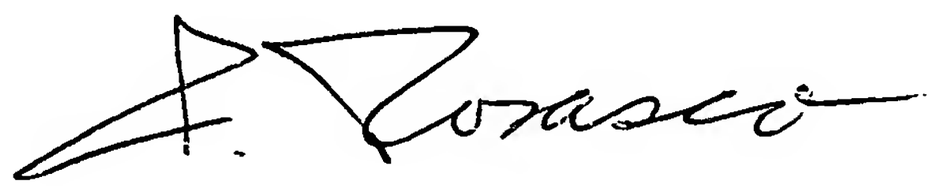
And wherein the feature having a critical width along a length thereof comprises a gate-shrink region of a transistor, and wherein the other feature is a diffusion region of a transistor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



S. Rosasco
Primary Examiner
Art Unit 1756

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09/05/06